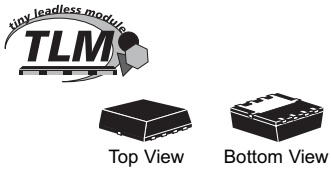
CTLT853-M833

SURFACE MOUNT
HIGH CURRENT
SILICON NPN TRANSISTOR
TINY LEADLESS MODULE™



Top View Bottom View

TLM833 CASE

MARKING CODE: CHA3
PNP COMPLEMENT: CTLT953-M833

Central™ Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLT853-M833 is a high performance 6.0A High Current NPN Transistor designed for applications where small size and operational efficiency are prime requirements. With a maximum power dissipation of 4.5W, and a very small package footprint, this device is 80% smaller than a comparible SOT-223 device. This leadless package design has a watts per unit area at least twice that of equivalent package devices.

FEATURES:

- High Voltage (200V)
- High Thermal Efficiency
- High Current (I_C=6.0A)
- 3 x 3mm TLM™ case
- Low $V_{CE(SAT)}$ = 340mV Max @ 5.0A

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	200	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Collector Current	I_C	6.0	A
Power Dissipation	P_D	4.5	W (Note 1)
Power Dissipation	P_D	4.0	W (Note 2)
Power Dissipation	P_D	2.5	W (Note 3)
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	27.78	°C/W (Note 1)
Thermal Resistance	Θ_{JA}	31.25	°C/W (Note 2)
Thermal Resistance	Θ_{JA}	50.00	°C/W (Note 3)

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	V_{CB}=150V			10	nA
I_{CER}	V_{CE}=150V, R_{BE} ≤ 1kΩ			10	nA
I_{CBO}	V_{CB}=150V, T_A=100°C			1.0	μA
I_{EBO}	V_{EB}=6.0V			10	nA
BV_{CBO}	I_C=100μA	200	220		V
BV_{CER}	I_C=10mA, R_{BE} ≤ 1kΩ	200	210		V
BV_{CEO}	I_C=10mA	100	110		V
BV_{EBO}	I_E=100μA	6.0	8.0		V
$V_{CE(SAT)}$	I_C=100mA, I_B=5mA		22	50	mV
$V_{CE(SAT)}$	I_C=2.0A, I_B=100mA		135	170	mV
$V_{CE(SAT)}$	I_C=5.0A, I_B=500mA			340	mV
$V_{BE(SAT)}$	I_C=5.0A, I_B=500mA			1.25	V

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 75 mm²
(2) FR-4 Epoxy PC Board with copper mounting pad area of 75 mm²
(3) FR-4 Epoxy PC Board with copper mounting pad area of 25 mm²

R0 (10-November 2006)

Central™
Semiconductor Corp.

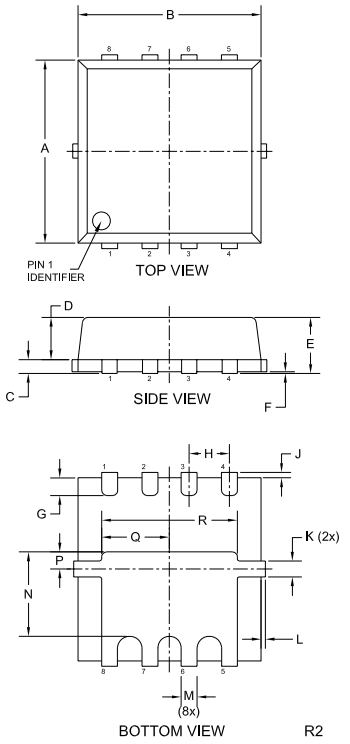
CTLT853-M833

SURFACE MOUNT
HIGH CURRENT
SILICON NPN TRANSISTOR
TINY LEADLESS MODULE™

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
h_{FE}	V_{CE}=2.0V, I_C=10mA	100			
h_{FE}	V_{CE}=2.0V, I_C=2.0A	100	200	300	
h_{FE}	V_{CE}=2.0V, I_C=4.0A	50	100		
h_{FE}	V_{CE}=2.0V, I_C=10A	20	30		
f_T	V_{CE}=10V, I_C=100mA, f=50MHz		190		MHz
C_{ob}	V_{CB}=10V, I_E=0, f=1.0MHz		38		pF

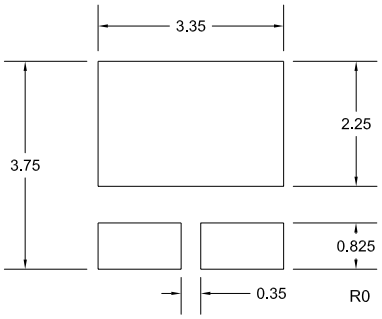
TLM833 CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.006	0.010	0.15	0.25
D	0.026	0.030	0.65	0.75
E	0.031	0.039	0.80	1.00
F	0.000	0.002	0.00	0.05
G	0.008	0.018	0.20	0.45
H	0.026		0.65	
J	---	0.005	---	0.125
K	0.007	0.012	0.17	0.30
L	---	0.005	---	0.125
M	0.011	0.015	0.29	0.39
N	0.049	0.057	1.25	1.45
P	0.006	0.014	0.15	0.35
Q	0.040	0.048	1.01	1.21
R	0.085	0.093	2.16	2.36

TLM833 (REV:R2)

Required Mounting Pad
(Dimensions in mm)



Failure to use this mouning pad layout may result in damage to device.

LEAD CODE:

1) EMITTER
2) EMITTER
3) BASE
4) N. C.
5) COLLECTOR
6) COLLECTOR
7) COLLECTOR
8) COLLECTOR

MARKING CODE: CHA3

R0 (10-November 2006)